Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech II Year I Semester Regular Examinations November 2019
DIGITAL LOGIC DESIGN
(CSE)

Time: 3 hours   Max. Marks: 60

PART-A
(Answer all the Questions 5 x 2 = **10** Marks)

1	a	State the associative property of Boolean algebra.	2M
	b	What are the 2 forms of Boolean expression?	2M
	c	Differentiate between encoder and decoder.	2M
	d	What is state diagram?	2M
	e	What are BIT, BYTE and WORD?	2M

PART-B
(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2 a Represent the decimal number 3452 in i)BCD ii)Excess-3.   5M
   b Perform (-50)-(-10) in binary using the signed-2's complement.   5M

OR

3 a Explain binary to Gray & Gray to binary conversion with example.   5M
   b State and Explain the DeMorgan's Theorem and Consensus Theorem.   5M

UNIT-II

4 Simplify the Boolean expressions to minimum number of literals   10M
i) $(A + B)(A + C')(B' + C')$
ii) $AB + (AC)' + AB'C (AB + C)$
iii) $(A+B)' (A'+B')'$

OR

5 Determine the minimal sum of product form of   10M
i) $f(w,x,y,z)=\Sigma m(4,5,7,12,14,15) +d(3,8,10)$.
ii) $F(A,B,C,D)=\pi M(0,3,5,6,8,12,15)$.

UNIT-III

6 a Implement the following Boolean function using 8:1 multiplexer   5M
      $F(A,B,C.D) = \Sigma m (0,1,2,5,7,8,9,14,15)$.
   b Explain about Decimal Adder.   5M

OR

7 Explain The Half adder and implement the full adder using two half adders.   10M

UNIT-IV

8 Explain the design of a 4-bit binary counter with parallel load in detail.   10M

OR

9 a Explain synchronous and ripple counters compare their merits and demerits.   5M
   b Design a 4-bit binary synchronous counter with D-flip flop.   5M

UNIT-V

10 Encode the 11-bit code 10111011101 into 15-bit information code.   10M

OR

11 Design PAL for a combinational circuit that squares a 3-bit number.   10M

END